Chapter

Digital On-Chip Calibration of Analog Systems towards Enhanced Reliability

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Abstract

This chapter deals with digital method of calibration for analog integrated circuits as a means of extending its lifetime and reliability, which consequently affects the reliability the analog electronic system as a whole. The proposed method can compensate for drift in circuit's electrical parameters, which occurs either in a long term due to aging and electrical stress or it is rather more acute, being caused by process, voltage and temperature variations. The chapter reveals the implementation of ultra-low voltage on-chip system of digitally calibrated variable-gain amplifier (VGA), fabricated in CMOS 130 nm technology. It operates reliably under supply voltage of 600 mV with 10% variation, in temperature range from $-20°C$ to $85°C$. Simulations suggest that the system will preserve its parameters for at least 10 years of operation. Experimental verification over 10 packaged integrated circuit (IC) samples shows the input offset voltage of VGA is suppressed in range of 13 μV to 167 μV. With calibration the VGA closely meets its nominally designed essential specifications as voltage gain or bandwidth. Digital calibration is comprehensively compared to its widely used alternative, Chopper stabilization through its implementation for the same VGA.

Keywords: on-chip digital calibration, PVT variations, aging compensation, reliability, input offset voltage, continuous operation, ultra-low voltage

1. Introduction

Every industry in our world shares the same fundamental motivation - packing as much functionality and power in the smallest possible size. This is naturally effective. In development of an integrated circuits fabrication technology, this trend is projecting in scaling down the minimum circuit element dimensions and circuit power supply voltage. In this way, higher performance and greater mobility is provided for electronic systems during their use. Such an advance, on the other hand, also introduces significantly increased random variations in circuit's electric specifications. The variations, in return, compromise the reliability already on the top level of electronic systems based on ICs as well as limit the functionality of circuits under constrained energy conditions. Deteriorated reliability of IC fabricated in modern nanotechnologies is significant not only between wafers and its series, but already within single die. Nowadays, ICs fabricated in 7 nm or 5 nm

process nodes can still perform well in digital signal processing. However, their analog counterparts substantially suffer from impaired reliability yet in 130 nm technology. This is of high concern with precise circuits such as operational amplifier (OA), which is usually based on differential topology. Occurrence of any differences in its differential branches, which might be a result of random variations, simultaneously induce degradation of the amplifier key parameters. In terms of circuit electrical parameters, these variations are mirrored by transistor's threshold voltage (V_{TH}). The V_{TH} variance is commonly characterized by standard deviation in the matched transistor pair with respect to its size as follows:

$$\sigma(\Delta V_{TH}) = \frac{A_{VTH}}{\sqrt{W.L}}, \tag{1}$$

where A_{VTH} is Pelgrom's technology coefficient, and W and L is the width and length of the transistor, respectively. The plot in **Figure 1** displays ΔV_{TH} for different process nodes according to works [1–5]. One can observe that downscaled process nodes suffer from much greater variance in V_{TH} with the change of device dimensions. In relative terms, the V_{TH} variance in 45 *nm* process node can reach 16% of mean value according to [6].

The adverse variations can be classified as rather acute - process, voltage and temperature variations, or they can occur after long term use as a consequence of electrical stress. The work [7] thoroughly analyzed the roots of these variations in a transistor as the fundamental IC element.

The following section describes the motivation behind our research. Section 3 explains the design details of the calibration methods implemented in this work. These include digital calibration (DGC) that was experimentally prototyped on a

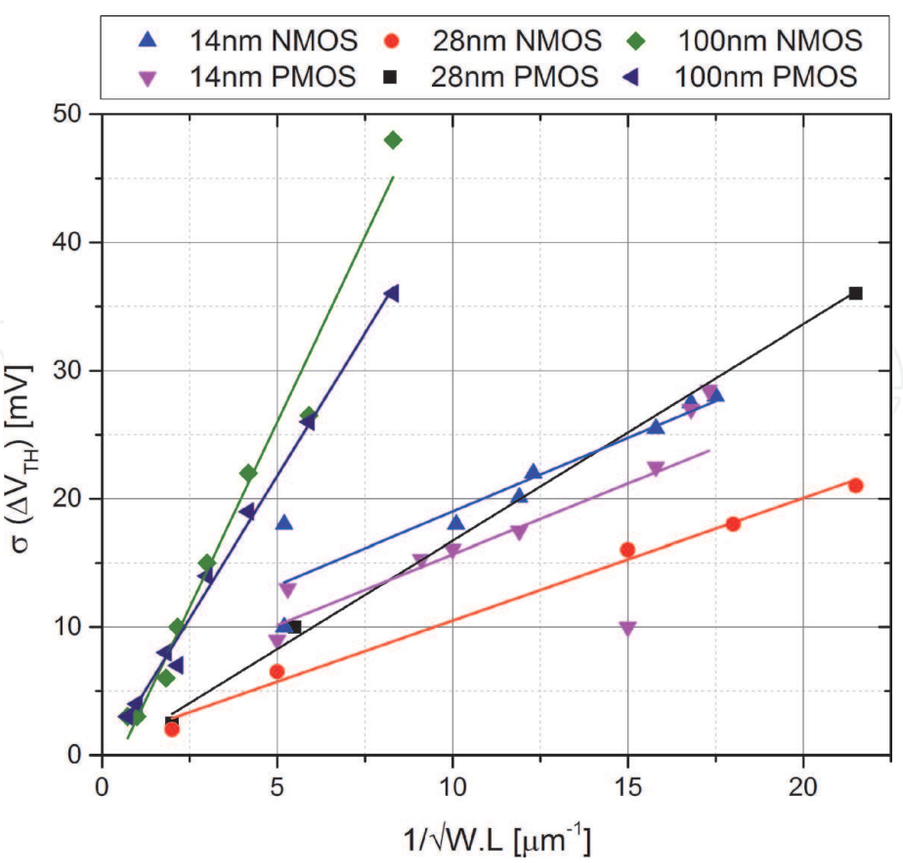

Figure 1.
Standard deviation of threshold voltage in matched transistor pair with respect to its size across different process nodes.

chip, its upgraded and optimized version (DGC2) and Chopper stabilization (CS) technique. Section 4 reveals results of extensive measurements and simulations of the proposed solutions. Finally, the Conclusion summarizes the most important outcomes of the presented research.

2. Motivation

Concluding the discussed state of the art, it is of high importance and it will be increasingly important in the future to compensate for stochastic variations in ICs to maintain reliable circuit operation. The parameter of an OA that is directly tied to any detrimental change in the transistor V_{TH} is the input offset voltage V_{INOFF}. It is therefore, an effective target of any calibration method. Among widely utilized techniques of IC calibration belong fuse trimming (one time or re-programmable), Chopper stabilization and auto-zero (AZ) technique.

In our work, we propose a promising alternative approach based on digital algorithm, that was utilized for the variable gain amplifier. It is fully integrated on-chip system, which is potentially entirely autonomous. This method creates moderate area and energy consumption overhead, but it preserves frequency performance of the calibrated VGA. The methods of calibration substantially differ in fundamentals of operation, which makes the comparison between them difficult. Therefore, we implemented also the CS method for the same VGA. In this way, we can precisely compare the digital calibration to an alternative solution in terms of implementation details.

3. Implementation of calibration methods

This section proposes an insights into design fundamentals of implemented methods of calibration. The fabricated system of DGC, its optimized version for continuous systems and CS will be analyzed. All methods are designed consistently in order to achieve a clear and relevant comparison. They are implemented in standard CMOS 130 nm process node and operate under the supply voltage of 600 mV. Each method was utilized for the same VGA, which was previously realized in the same technology. The calibration is based on compensation of V_{INOFF} the designed and manufactured VGA exhibits. The VGA is nominally designed to reach DC gain magnitude of 33 dB with bandwidth of 17 kHz with capacitance load of 10 pF.

3.1 Fabricated system of DGC

Figure 2 depicts the block structure of digitally calibrated VGA, which has already been fabricated and evaluated. The calibration subcircuit connects to VGA through sensing ($P_{S1,2}$) and compensation ($P_{C1,2}$) ports. These are followed by the control and compensation blocks of the calibration subcircuit.

The control block senses the actual V_{INOFF} through the voltage comparators, as it is tied to output offset voltage with the following formula:

$$V_{OUTOFF} = A_{CLG}.V_{INOFF}, \tag{2}$$

where V_{OUTOFF} is the output offset voltage and A_{CLG} is amplifier's closed-loop gain.

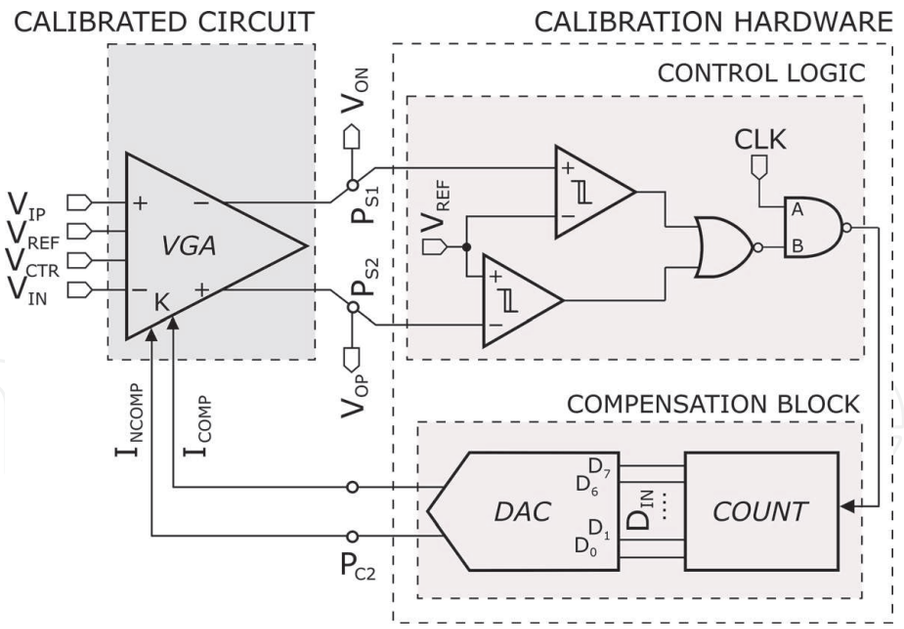

Figure 2.
Implementation of digital calibration for VGA input offset voltage cancelation.

The compensation block is connected to VGA topology so it can modify the current flow in its differential branches. As long as VGA outputs ($V_{OP,ON}$) do not cross the reference voltage (V_{REF}) at comparators' inputs, the digital-to-analog converter (DAC) adjusts the currents in the VGA. These currents are proportionally projected to V_{INOFF}. When either one of VGA outputs crosses the V_{REF}, the corresponding comparator terminates the clock signal, which drives the compensation block. In this way, V_{OP} and V_{ON} are brought close to each other, diminishing the offset voltage.

The direct schematic detail of compensation port is depicted in **Figure 3**. In this configuration, the DAC output current is mirrored to VGA through the active load of the amplifier, transistors M_{P1} and M_{P2}. The current mirror is formed by transistors M_{Z2}, M_{Z3}, M_{Z5} and M_{Z6}. The current mirror on the side of VGA is connected in bulk-driven configuration, which is specific by using the substrate electrodes to control the transistor. The reason for using this topology is better matching in drain-source voltage of mirroring devices M_{Z5} and M_{P1} (analogically M_{Z6} and M_{P2} for the other VGA branch), as their gate and substrate electrodes are correspondingly tied together. Also the bulk-driven topology performs better in low-voltage conditions

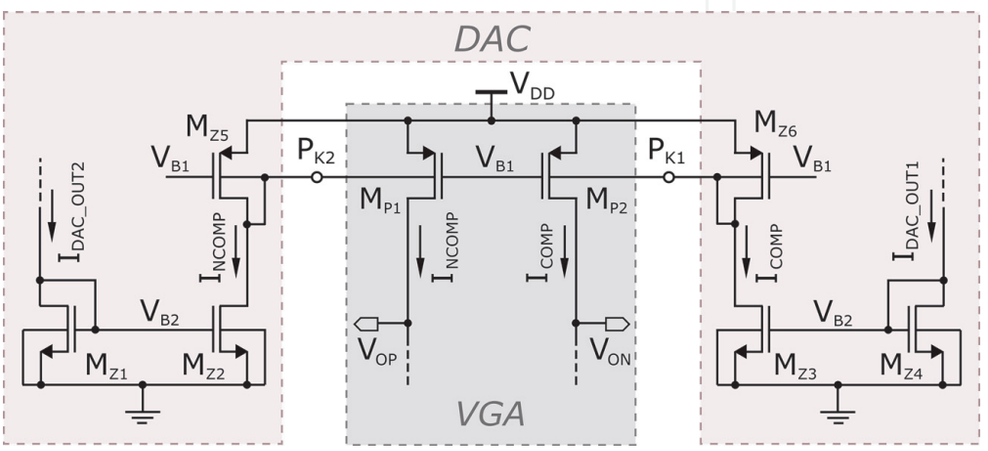

Figure 3.
The detail of compensation port at schematic level. This represents interface between DGC and VGA.

of the designed system, as it allows to modify the. This is clear from the following formula:

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right), \tag{3}$$

where V_{SB} is the bulk electrode voltage, V_{TH0} is threshold voltage at $V_{SB} = 0V$, γ is the body effect coefficient and Φ_F is the Fermi potential.

The layout of complete DGC system is depicted in **Figure 4**. The main blocks are highlighted from the principle structure point of view from **Figure 2**. The dimensions are shown in μm. The VGA covers 18500 μm^2, while the DGC circuits together take 19000 μm^2 without the optional trimming fuses.

Figure 5 displays the micrograph of an experimental chip prototype, where the digital calibration system is marked.

3.2 Optimized system of DGC for continuous operation

As it was described in the previous section, the voltage–current conditions in VGA are modified through the iterations of calibration cycle. The VGA is imbalanced in this process and therefore, cannot perform its intended function.

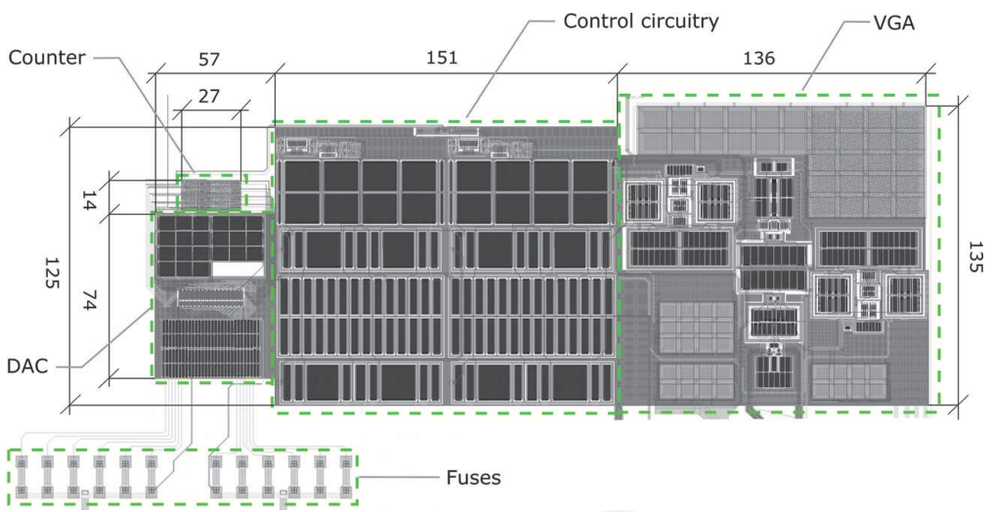

Figure 4.
The layout of the whole calibration system (dimensions in μm).

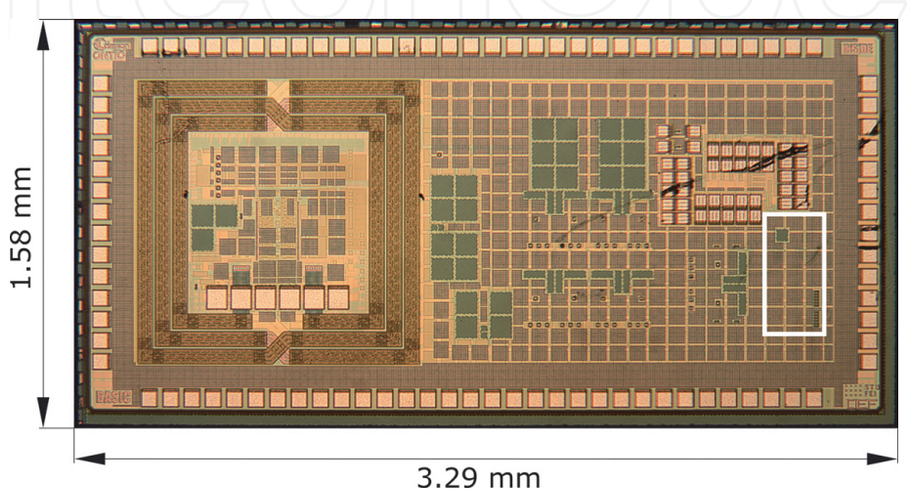

Figure 5.
The micrograph of die with marked area of implemented DGC.

In systems without the need to continuously process the signal, this does not represent an issue, since through proper synchronization the calibration cycle it can be carried out during idle phase. To utilize the digitally calibrated VGA in an application requiring continuous operation, the technique called "Ping-pong" facilitates the necessary continuity [8, 9]. Its principle can be illustrated by the block diagram shown in **Figure 6**. It uses the calibrated VGA in two identical versions, where the one (VGAX) provides the amplified output while the other (VGAY) is calibrated. When the circuit characteristics change due to temperature or voltage variations, both amplifiers switch their roles. In this way, the output is provided only by already calibrated VGA.

To explain the operation of "Ping-pong" digital calibration (PDGC) more clearly, **Figure 7** shows exemplary transient flow of the operation on key signals of system in **Figure 6**. The temperature change in this example, creates the conditions, in which the calibration is required. During the system initialization, the VGAX is calibrated and its output offset voltage ($V_{OUTOFFX}$) is suppressed to a range of hysteresis ΔV_{HYST}. The overall system output (V_{OUT}) is consequently switched to VGAX in time t_0. When the V_{INOFFX} drifts above ΔV_{HYST} with temperature, the calibration of VGAY begins in time t_1. When the calibration cycle is completed, the signal SW_Y indicates it by a rising edge and the output of VGAY is switched to V_{OUT} in time t_2. In this way, the phases of PDGC are autonomously interchanged according to temperature, which is evaluated by a temperature sensor. The maximum overall output offset voltage at V_{OUT} is maintained nearly above ΔV_{HYST} without any substantial corruptions.

During switching VGA versions, the V_{OUT} can suffer from voltage spikes. These produce significantly smaller artifacts of frequency spectrum than spikes resulting from charge injection present in switched calibration methods such as auto-zero technique. Also the spikes can be eliminated by incorporating transfer phase, when the calibrated amplifier is firstly connected as a buffer before being fully switched to the system output [8].

Utilization of "Ping-pong" technique required a few modifications to a system of digitally calibrated VGA in **Figure 2**. These are incorporated in its upgraded and optimized version, depicted in **Figure 8** with more insights into the control logic block shown in **Figure 9**. In this modified system, the power-on-reset (POR) circuit is present, which is controlled by *RPT* pin. The POR activates the calibration of idle

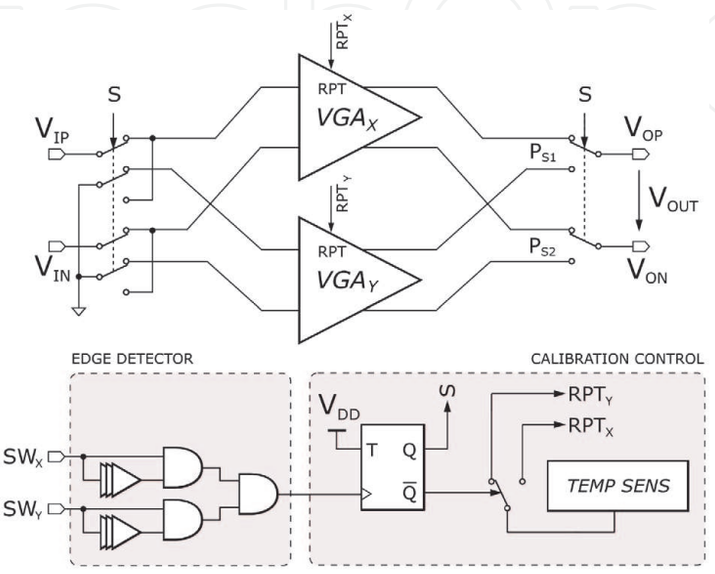

Figure 6.
The "ping-pong" technique for digitally calibrated VGA with continuous output.

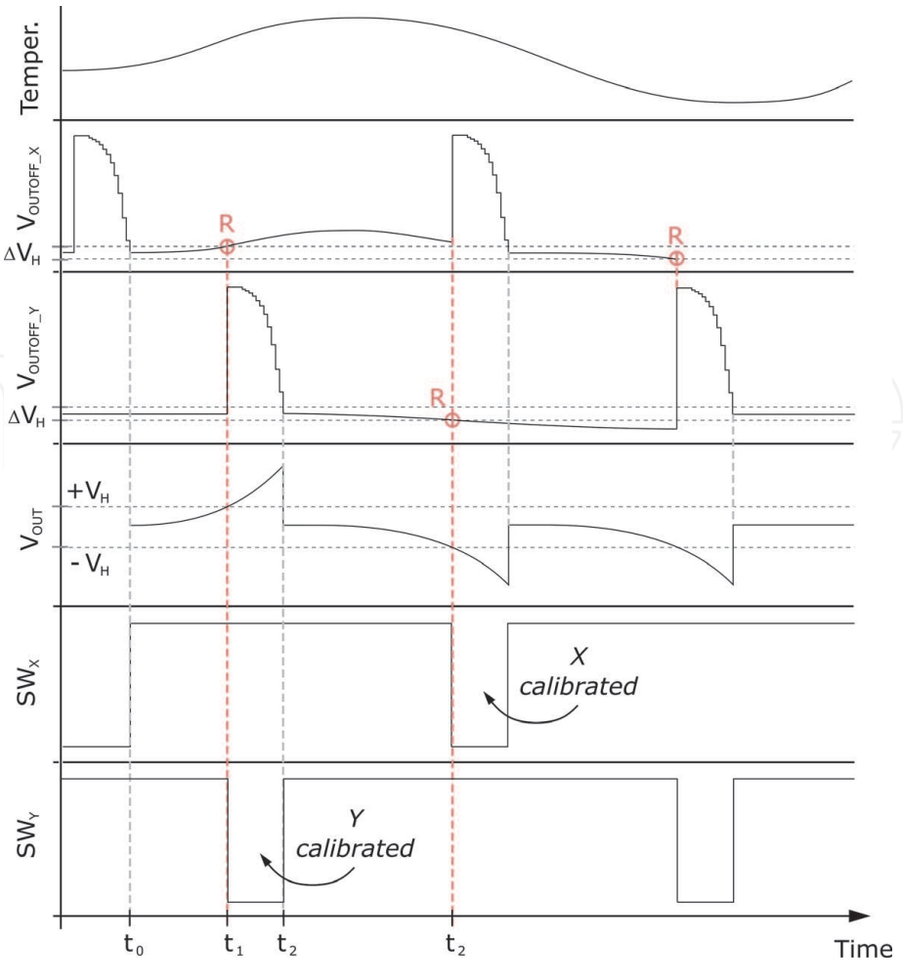

Figure 7.
The "ping-pong" technique for digitally calibrated OA with continuous output.

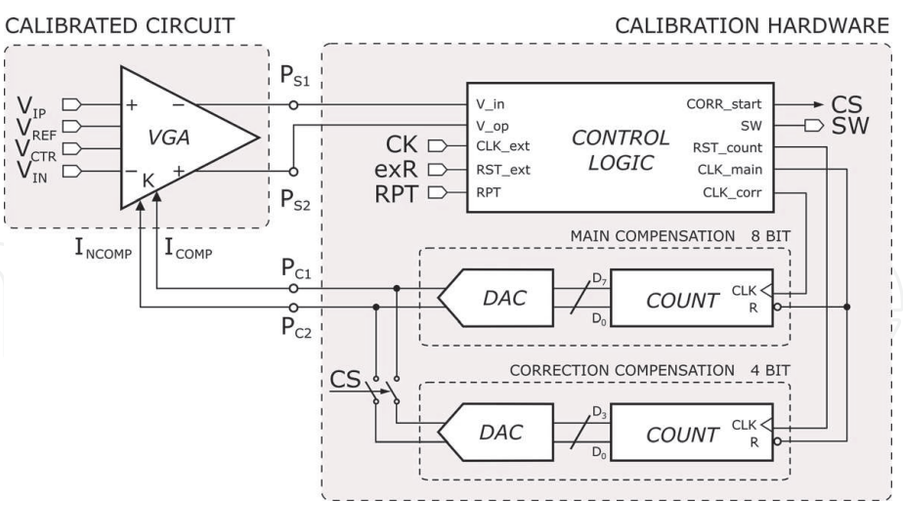

Figure 8.
The improved version of digitally calibrated VGA for integration into "ping-pong" method.

VGA, when it is required to be switched to the system output. Also the pin SW indicates the calibration cycle is completed. The new version of DGC depicted in **Figure 8** also incorporates modifications, which brings better overall efficiency of the discussed method. There is an additional 4-bit DAC, which corrects the residual offset remaining after the main calibration cycle has been completed. In this way, the magnitude of offset voltage is further suppressed. The two sensing comparators of the previous version are now replaced by a single one, which is much simpler

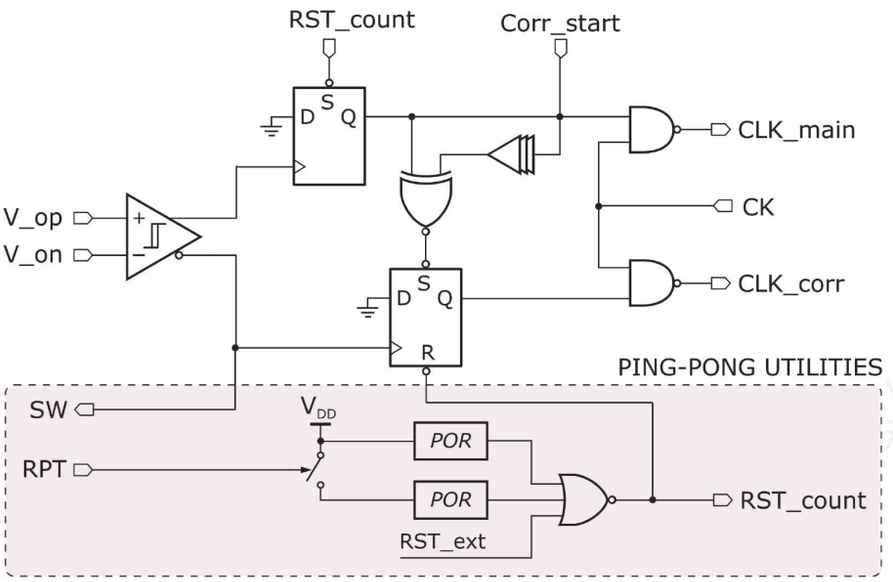

Figure 9.
Optimized control block for digital calibration with upgrades for "ping-pong" approach.

solution but with tighter specifications for a successful calibration. A D-type flip-flops in the control block terminate the distribution of *CLK* signal when the calibration is finished, which prevents unintended launch of another calibration cycle.

The optimized DGC from **Figure 8** covers only 6000 μm^2 instead of 19000 μm^2 taken by the original version. Also the power consumption of calibration circuits is lowered from 41μW to just 6μW, which is almost 7 times lower.

3.3 Chopper stabilization

In order to obtain precise comparison of calibration methods, so-called chopper stabilization has been utilized for the same VGA as in DGC, serving as an alternative method. In this way, the figure of merit (FOM) can be defined by considering the chip area coverage, power consumption and residual V_{INOFF}, as main parameters obtained over sufficient number of samples. The proposed chopper stabilization has been build according to the basic principle, without complex techniques, which would require an auxiliary amplifiers.

The block diagram of chopper-stabilized VGA is shown in **Figure 10**. It consists of modulator and demodulator employed at the VGA input and output, respectively. These are switched by signal $m(t)$ with frequency of 20 *kHz* so that it falls in VGA bandwidth. In order to make the comparison to DGC objective and relevant, we established the limit for total harmonic distortion (THD) at the value of 1%. The output of demodulator provides the carrier signal $m(t)$ with the envelope formed by V_{IN}. Therefore, the low-pass filter needs to be employed at each output channel. As there are requirements for low THD and low corner frequency (f_c) of 10 *kHz* (suppressing $m(t)$), the filter must incorporate significantly large values of capacitor

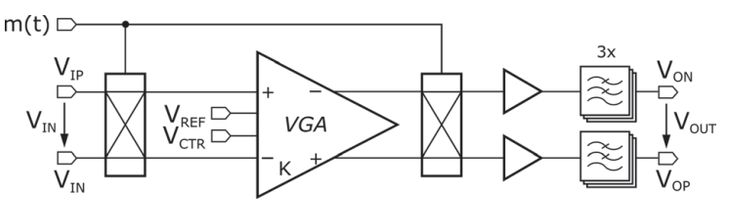

Figure 10.
The block diagram of chopper-stabilized VGA.

and resistor. Moreover, the f_c needs to be as close as possible to $m(t)$ frequency, so that the filter cuts the smaller portion of overall VGA bandwidth. To meet this requirement, the filter needs to reach significant steepness or in other words, the order. The mentioned specifications demand rather complex solution consisting of a frequency filter with large values of passive components. It was realized as Sallen-Key active filter of 2^{nd} order, which is used 3 times in series for each VGA output channel. These two pairs of the filter cover together approximately 800 000 μm^2. While the VGA occupies only 18 500 μm^2, using the CS in this conditions would create a tremendous area overhead.

The large silicon area covered by frequency filters can be mitigated by switched capacitors that are used instead of classic resistors. On the other hand, the switching frequency in this case, would demand yet another design solution to maintain a low distortion of the processed input signal.

4. Verification

Fabricated system of DGC, described in section 3.1 was experimentally verified. The measurements have been carried out on 10 packaged IC samples at the ambient temperature of 27°C. All implemented methods of calibration for VGA were extensively verified through simulations in Cadence environment. These included process corner analysis, Monte Carlo (MC) and RelXpert reliability analysis. Each simulation type has been carried out in the temperature range from −20°C to 85°C. MC was performed with 150 sample scenarios. Reliability analysis simulates the operation of an IC after initial electrical stress and operation after 10 years of stress. It is based on the bias temperature instability (BTI) and hot carrier injection (HCI), the phenomena which gradually degrade the IC reliability and dependability. It does not consider time dependent dielectric breakdown since this is rather acute in nature. Reliability analysis considered simultaneously the process corners and geometry mismatch as well.

In order to optimally design the calibration circuits, the experimental measurements of V_{INOFF} in the same VGA without calibration (previously fabricated) hardware were performed. Measurements were carried out on 60 naked dies. The resulting offset distribution is displayed in **Figure 11** and compared to MC result distribution. 3σ range of V_{INOFF} reaches approximately 10 mV. Hypothetically, with

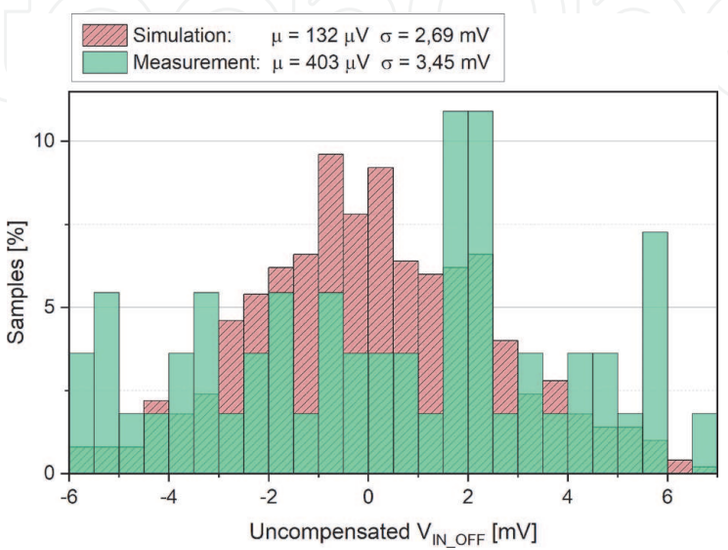

Figure 11.
Distribution of V_{INOFF} of uncalibrated VGA. Comparison of experimental measurements and MC analysis.

the VGA nominal gain of 33 dB such V_{INOFF} would project to 460 mV in the differential output voltage. Considering the VGA being supplied by 600 mV, its outputs would reach almost to the supply rails range even in the optimum operating point.

Histograms depicted in **Figures 12–14** compare the MC simulation results of V_{INOFF} of digitally calibrated VGA, chopper-stabilized VGA and VGA without a calibration. The achieved results prove a comparable performance of DGC and CS in terms of standard deviation, while CS reaches better centering of distributions towards 0 V. Both methods of calibration successfully suppress the V_{INOFF} in magnitude of orders through the whole temperature range.

Figure 15 displays the transient flow of digital calibration cycle through the VGA output voltages. It compares the best and worst case scenarios of technology process corners after the initial stress and after 10 years of operation. After the calibration is successfully completed, the VGA is fed the harmonic signal of 0.5 mV differential amplitude and frequency of 1 kHz. The detail of plot in right-hand side part of **Figure 15** zooms the differential output voltage of the calibrated VGA in proper operation. The calibration cycle was controlled by clock signal with frequency of 1 kHz. **Figure 16** displays the measured flow of calibration cycle also through VGA

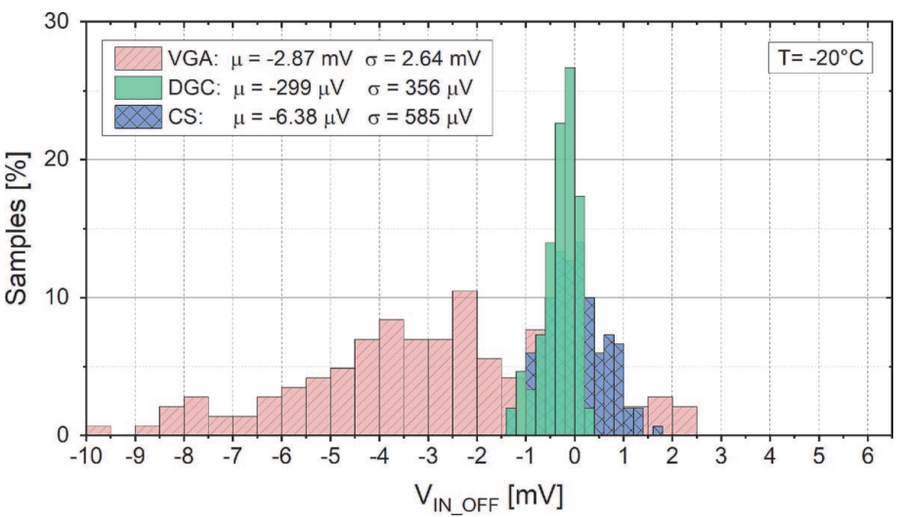

Figure 12.
MC simulation results of V_{INOFF} in digitally calibrated VGA, chopper stabilized VGA and VGA without calibration. Temperature of −20 C.

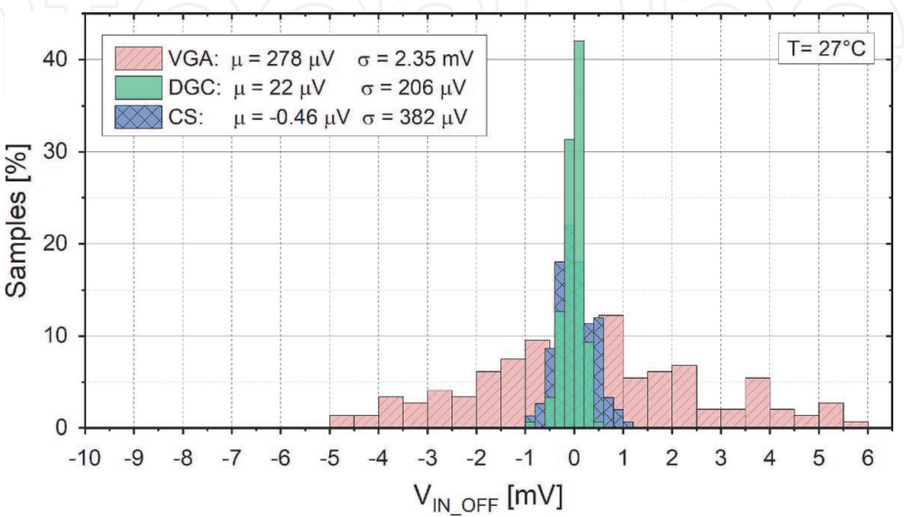

Figure 13.
MC simulation results of V_{INOFF} in digitally calibrated VGA, chopper stabilized VGA and VGA without calibration. Temperature of 27°C.

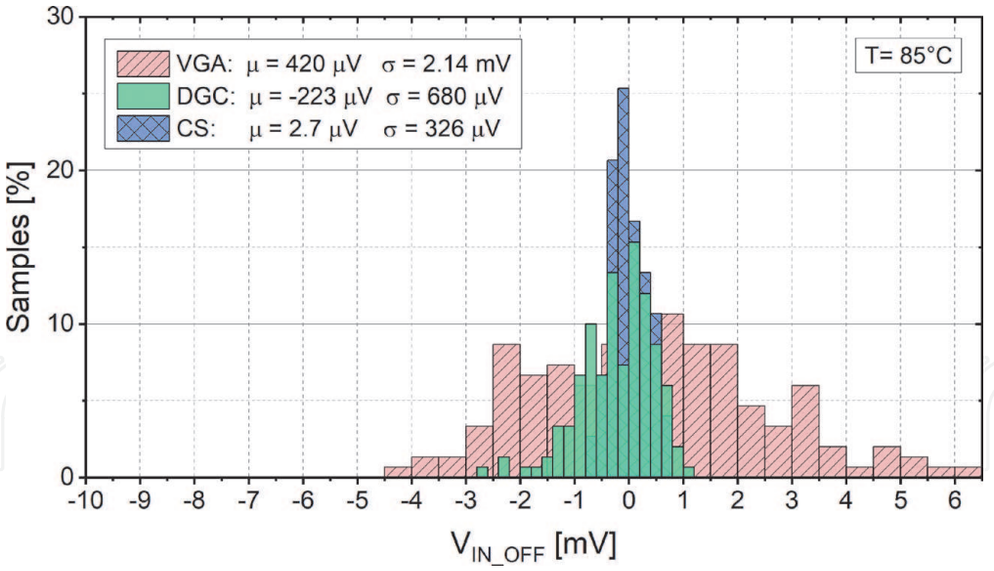

Figure 14.
MC simulation results of V_{INOFF} in digitally calibrated VGA, Chopper stabilized VGA and VGA without calibration. Temperature of 85°C.

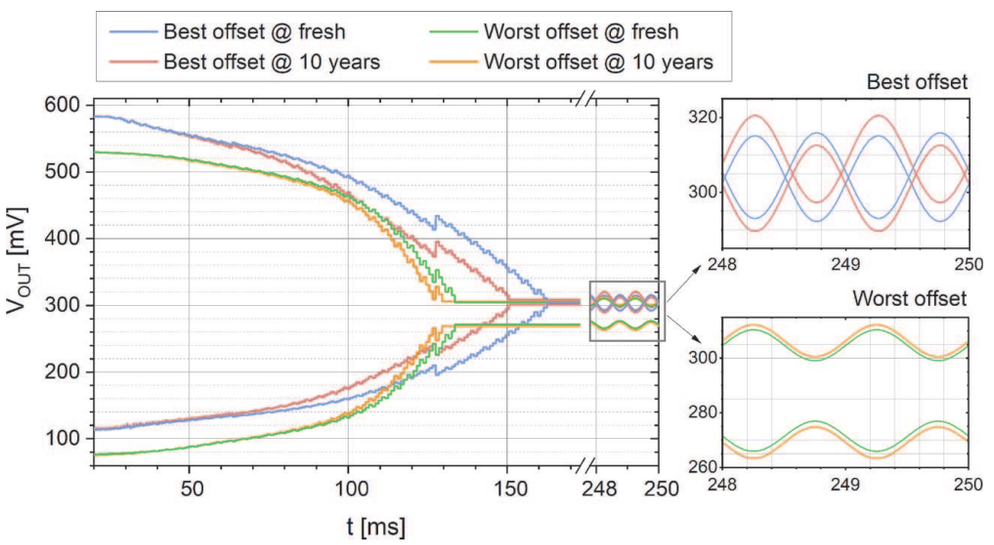

Figure 15.
Reliability analysis of digitally calibrated VGA considering process corners and geometry mismatch. The calibration cycle at fresh IC is compared to the IC of 10 years of age.

output voltages. The best and worst cases of the measurement and simulation results are compared. The calibration was performed with CLK frequency of 350 *kHz*. The whole cycle from beginning to the point where VGA is ready for proper operation lasts between 210 *μs* and 319 *μs*. **Figure 17** compares the gain of VGA obtained by measurement and simulation in the best and worst cases. Measurements were carried out using the maximum input signal amplitude for VGA, which allowed to keep the total harmonic distortion under 1%. As one can observe, the experimental results fit the simulations very well. The upgraded, more precise DGC version, described in section 3.2 is actually being re-designed at the moment. **Figures 18–20** compares the MC simulation results of V_{INOFF} to the prototype version over the industrial temperature range. The mean value of offset is compensated in one order of magnitude further towards 0 *V* by means of new DGC. Standard deviation remains approximately constant. The reason behind it is supposed to be the offset voltage of sensing comparator in DGC. It causes premature termination of main calibration cycle, which alone produces excessive residual V_{INOFF}. Consequently, the issue is amplified

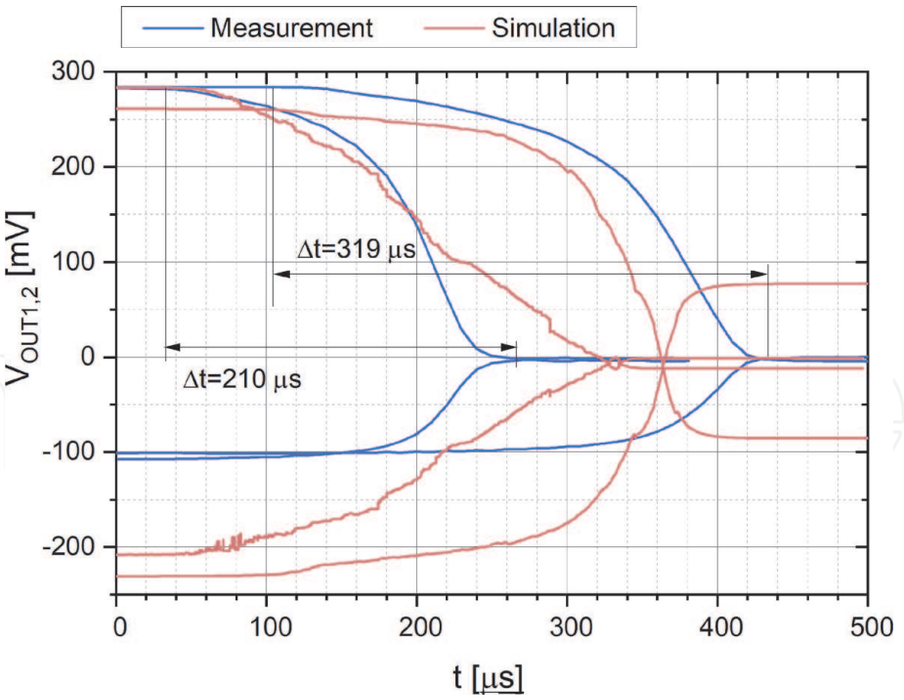

Figure 16.
Transient flow of the calibration cycle. The comparison of the best and the worst case of measurement and simulation.

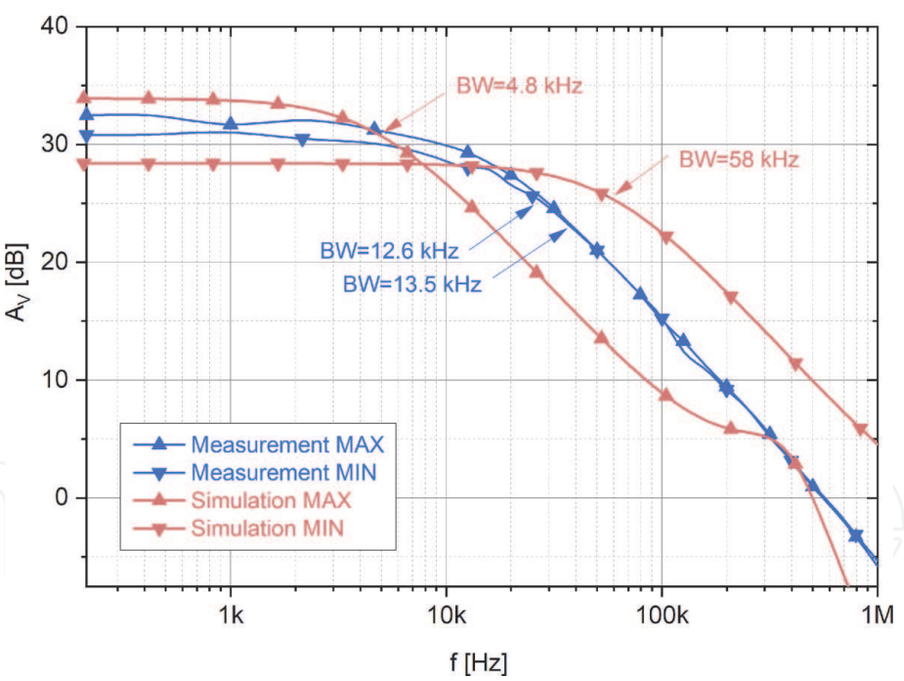

Figure 17.
Measured vs. simulated gain of the digitally calibrated VGA.

because faulty termination launches correction calibration cycle in the wrong direction, enhancing the residual V_{INOFF} even further. On the other hand, this shortcoming of upgraded DGC can be easily resolved by auto-zeroing the sensing comparator. As it processes discontinuous signal (proportional to DAC output), the proper synchronization of switching the AZ sample phase with CLK of calibration would preserve the overall DGC progress untouched.

Table 1 summarizes the most important results of calibration methods, implemented in this work. There are compared measurement and simulation results

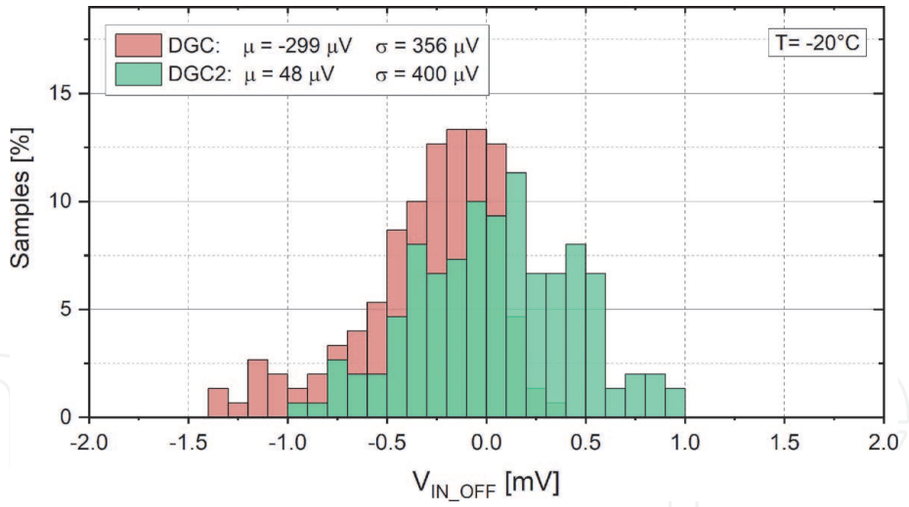

Figure 18.
Measured vs. simulated gain of the digitally calibrated VGA for temperature of −20°C.

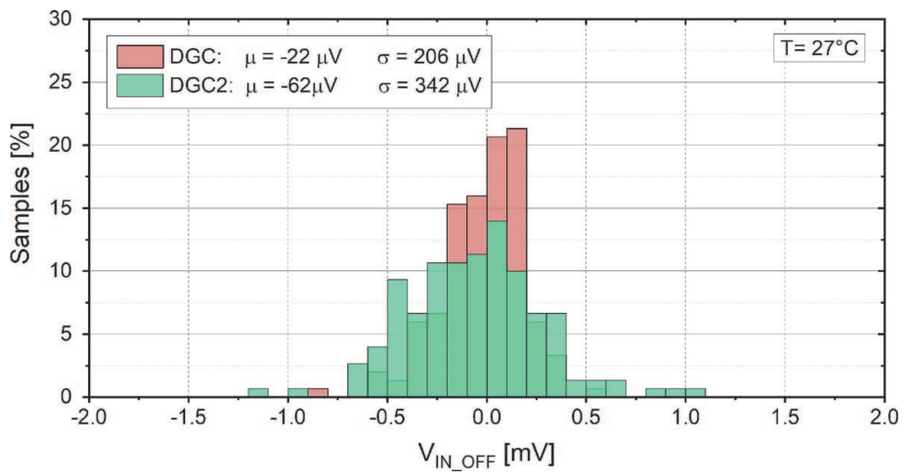

Figure 19.
Measured vs. simulated gain of the digitally calibrated VGA for temperature of 27°C.

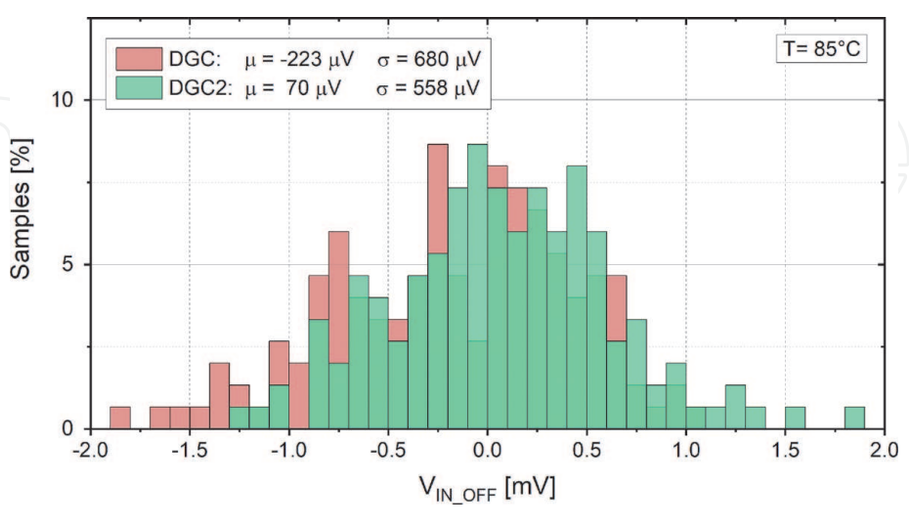

Figure 20.
Measured vs. simulated gain of the digitally calibrated VGA for temperature of 85°C.

of prototype DGC version and simulation results of upgraded DGC (DGC2) and CS. The whole data were obtained at room temperature of 27°C for the purpose of comparison to related works shown in **Table 2**. As all details in these designs were

		DGC				DGC2[3)]		CS	
		min	**max**	μ	σ	μ	σ	μ	σ
Year		2020							
Node	$[nm]$	130							
$\mathbf{V_{DD}}$	$[V]$	0.6							
$\mathbf{S_{OA}}^{1)}$	$[.10^3 \mu m^2]$	18.4							
$\mathbf{S_{CH}}^{2)}$	$[.10^3 \mu m^2]$	19				6		800	
$\mathbf{P_{OA}}^{1)}$	$[\mu W]$	—	—	38	3	38.5	3.6	30.4	3.1
$\mathbf{P_{CH}}^{2)}$	$[\mu W]$	—	—	41	6.1	5.6	0.7	62.7	11
$\mathbf{V_{INOFF}}$	$[\mu V]$	13	167	22	206	18.5	390	2.75	95
THD	[%]	1		0.04	0.02	0.83	0.07	0.05	0.03
$\mathbf{A_{DC}}$	$[dB]$	31	33	35.3	2.7	33.6	8.2	30.23	2.2
BW	$[kHz]$	12.6	13.5	15.25	2.2	15.9	2	0.9	—
GBW	$[MHz]$	0.6		0.75	0.06	800	61	3	—
FOM	$[-]$	**—**		**41**		**340**		**4**	
Results		Meas.				Sim.			
Calibration		Dig.						Chop.	

[1)] *Chip area coverage (S) and power consumption (P) of the calibrated OA.*
[2)] *Chip area coverage (S) and power consumption (P) of the calibration hardware.*
[3)] *Upgraded and optimized version of the prototyped DGC.*
Bold values are emphasize the parameter FOM, which is one of most important results in this work.

Table 1.
The main results of the proposed calibrated systems.

accessible, the figure of merit (FOM) has been determined according to the following formula:

$$FOM = \frac{1000}{\mu(V_{INOFF}).A.P} \tag{4}$$

where the parameters are:

- $\mu(V_{INOFF})$ - mean value of residual input offset voltage after calibration over sufficient number of samples,
- $A = A_{CH}/A_{CC}$ - ratio of calibration hardware die area versus area of calibrated circuit,
- $P = P_{CH}/P_{CC}$ - power consumption of calibration hardware versus power consumption of the calibrated circuit.

The FOM value evaluates the power and area efficiency of the obtained calibration result over a sufficient number of samples. Its coefficients are in denominator, and therefore, the greater value of FOM proves better overall performance of calibration method. The value of coefficients is multiplied by 1000 in numerator to shift the results into the order of tens to thousands. The crucial condition for objectivity in this comparison is the THD of the amplifier is maintained under 1% at any method of calibration.

		This work		[11]	[12]	[13]	[14]	[10]
		μ	σ					
Year		2020		2015	2008	2008	2010	2013
Node	$[nm]$	130		130	350	180	130	130
$\mathbf{V_{DD}}$	$[V]$	0.6		1.2	1	1.8	1.2	2.8
$\mathbf{S_{OA}}$ [1)]	$[.10^3 \mu m^2]$	18.4		12.3	224	36	34	630
$\mathbf{S_{CH}}$ [2)]	$[.10^3 \mu m^2]$	6		12.3	17.4	30	33.2	261
$\mathbf{P_{OA}}$ [1)]	$[\mu W]$	38.5	3.6	13920	7900	11000	2000	156800
$\mathbf{P_{CH}}$ [2)]	$[\mu W]$	5.6	0.7				2400	
$\mathbf{V_{INOFF}}$	$[\mu V]$	62	342	5	σ=538	126	75	0.097
THD	[%]	0.83	0.07	—	0.01[3]	0.4	—	—
$\mathbf{A_{DC}}$	$[dB]$	33,6	8,2	0–60	−22 - 30	−6 - 58	32	90
BW	$[kHz]$	15.9	2	250000	17000	22000	57000	40000
OA stages		1		4	3	3	1	1
FOM	$[-]$	**340**		**205**†	**24**	**10**	**11**†	**25 000**†
Results source		Sim.		Meas.	Sim.	Meas.	Meas.	Meas.
Calibration method		Dig.		Analog.	Analog.	Dig.	Analog.	Dig.

[1)] Chip area coverage (S) and power consumption (P) of the calibrated OA.
[2)] Chip area coverage (S) and power consumption (P) of calibration hardware.
† These works does not contain information about THD, therefore the comparison is not fully relevant.
Bold values are emphasize the parameter FOM, which is one of most important results in this work.

Table 2.
The results comparison of the proposed work to related works.

It is obvious that CS outperforms even DGC2 in term of V_{INOFF}. It maintains the nominally designed low-frequency gain (A_{DC}) at 30.23 dB. On the other hand, the bandwidth (BW) is seriously constrained due to extensive filtering and the principle of CS alone.

However, this is not an issue with DGC and DGC2 approach, as the simulation results of BW after the calibration converge on the nominally designed 17 kHz. The measurement value of BW exhibits a certain decline, which could be assigned to

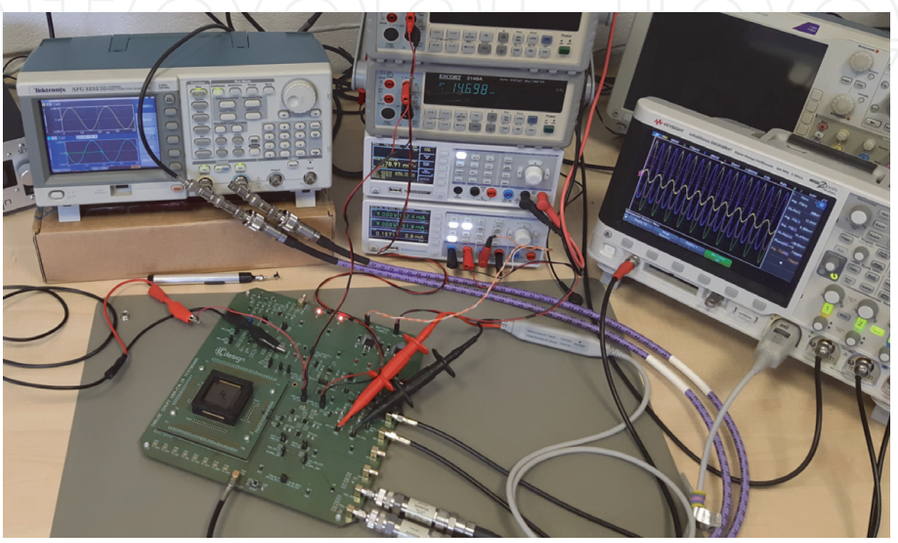

Figure 21.
The automated measurement setup for evaluation of the prototype calibrated systems.

parasitic capacitances associated with measurement setup, as well as to the measurement error due to small signal amplitude. Thanks to optimization of occupied silicon area and power consumption the DGC2 outperforms CS according to FOM. **Table 2** compares the proposed results to related works in the scientific area. This comparison was problematic as the calibration methods are most often built in more complex systems as DBS receiver circuit [10] and others. They are therefore side topics and authors do not mention the details, which are critical in terms of calibration. One such limitation is missing the level of THD, which sets equal conditions with calibration methods, presented in this chapter. The FOM values proves DGC2 for being a competitive solution for calibration of analog integrated circuits.

Figure 21 depicts the setup for automated measurements, which served for the evaluation of prototype chips.

5. Conclusions

Prevalent trends in IC fabrication reveal an increasing sensitivity to process, voltage, temperature variations and aging that projects directly into degradation of the overall perfomance of integrated systems. While digital systems are proven to be robust enough to above mentioned fluctuations even below 10 *nm* process node, their analog counterparts suffer from significantly decreased yield already in 130 *nm* technology node. This is confirmed by an actual research and also by experimental results provided within this chapter. Various methods of calibration have been presented and proven to effectively aid analog integrated circuits in preserving their reliability. These methods are rather complex, which constricts them for very specific use. This chapter extensively analyses the digitally controlled calibration method aimed at compensating the input offset voltage of the variable-gain amplifier. Chopper stabilization technique was implemented for the same amplifier, ensuring an objective comparison. Digital calibration was verified by simulations and experimental measurements on a prototype chip, which uniformly proved the reliable performance of the calibrated system. The established figure of merit shows that digital calibration represents an effective solution for preservation of reliability level in continuous systems with low distortion. The proposed method operates with lowest supply voltage level and also achieves the lowest silicon area and power consumption between the compared solutions, while maintaining competitive level of the calibrated input offset voltage. The area, which is added by calibration hardware can be mitigated by relieving demands for robustness of the calibrated circuit. By means of digital processing the method itself is robust against electrical variations.

Concluding the provided results, the digital calibration proves to be a promising solution in aiding the analog ultra-low voltage systems on chip towards a reliable operation, which is enormous challenge in modern nanoscale technologies. The proposed method is area and power efficient, while its operation remains stable over at least 10 years life span. It can be easily integrated along the calibrated circuit on a single chip in deep sub-micron process nodes. Taking into account the further research, it can become fully autonomous. In this way, the handling of calibrated circuit remains intact of calibration management.

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